Peak-Power Resistive Products

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Introduction 2
Construction of High Power Resistors 2
Methods for Testing High Power Resistors 5
Power Specification and Derating 8
Method to Determine θjb(max) 9
DC Power vs. RF Power 9
Pulse Power Stress 10
Pulse Power Testing 13
Summary 14

Introduction

Evolving market requirements are demanding a higher level of performance from resistive products. Aside from the challenge of dissipating higher power levels in a smaller footprint, passive components must also operate under high peak-power stresses. As radio detection and ranging (RADAR) becomes more prevalent in various industries, including the commercial sector, peak power requirements will continue to evolve and hopefully at some point become standard. In addition to today's traditional RADAR applications, many modern communication applications exploit various properties of burst transmission, which can have significant peak power levels requiring processing. This requirement has generated a market need for passive products designed and manufactured specifically to dissipate high-peak power events, for the life of the product.

The objective of this paper is to describe high-power test methodologies as related to Florida RF Labs resistive products, with an emphasis on pulsed power. This paper will provide a primer on high power passive product construction, specification and test methodologies for acceptance.

Construction of High Power Resistors

Understanding the design goal of high power resistors starts with knowledge of the entire resistor assembly as well as the dissipation mechanism of the resistor. An exploded cross sectional view of a flanged termination such as Florida RF Labs part number 32-1123 is depicted in **Figure 1**. A termination is simply a resistor (typically 50 Ω) with one terminal shorted to ground. (For this paper, the term "resistor" and "termination" will be use interchangeably throughout this paper considering the same thermal principles apply for both.) The mounting plate to which the termination will be grounded to, both electrically and thermally, is also found in **Figure 1**. The drawing is not drawn to scale and is intended to be used as a reference. Both the function and material configurations of each BOM item in **Figure 1** is outlined in **Table 1**.

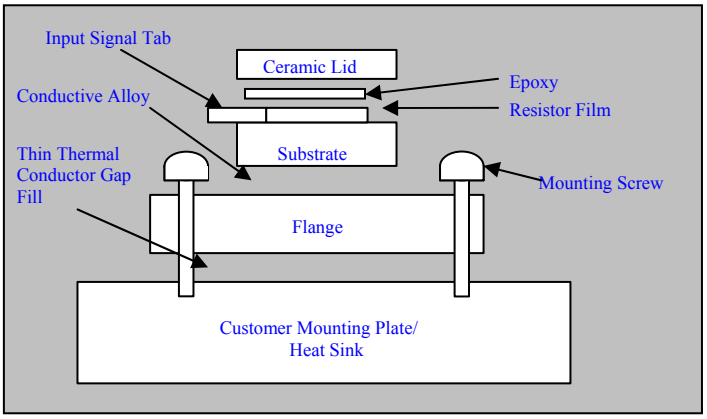

Figure 1: Cross section view of a flange mounted resistor

An open view of the resistor assembly can be seen in **Figure 2** where the ceramic lid and epoxy are removed from the assembly to expose the heart of the resistor assembly: the active resistor area. This resistor area (A cm^2) is the dissipative element which converts electrical/RF energy to thermal energy/heat. In general, larger active resistor areas have the ability to dissipate high levels of power. To ensure optimum performance, a low

Piece Part	Purpose	Typical Material
Customer Mounting Plate	Low thermal resistance mounting surface	Customer Specific
Thin-Thermal conductive gap fill	Fill small voids between flange and customer mounting plate to achieve best thermal transfer	Thermal grease
Mounting Screw	Provide force to ensure good thermal contact between flange and heat sink	Stainless Steel
Flange	Thermal spreading and ease of customer installation	Cu, CuW, Kovar, Al Various alloys and platings
Conductive Alloy/Bond	Attach ground plane of substrate to flange	SN62, SN96, AuSn, Epoxy
Substrate	Electrically insulative, thermal conductor	Al_2O_3, BeO, AlN, CVD Diamond
Resistor Film	Dissipate electrical energy as heat	Thin-Film, Thick-Film
Input Signal tab	Electrical interface between customer and dissipative resistor film.	BeCu, various platings
Epoxy	Adhere Ceramic lid to substrate	Non-conductive epoxy
Ceramic Lid	Protect resistor and captivate input signal tab. Safety feature and captivation mechanism.	Al_2O_3, BeO, AlN

Table 1: Piece part detail of Flanged Resistor

thermal resistance path from the resistive film to the customer mounting plate or heat sink must be maintained. For this reason, high thermally conducting, electrical insulators are utilized for high power products. Common dielectrics of choice used for high power applications are Beryllia, Aluminum Nitride and CVD Diamond.

As depicted in **Figure 1**, many components make up the termination assembly. In application, this assembly is mounted to a thermal sink. This thermal sink must have an adequate thermal capacity to ensure proper cooling of the assembly. Further, the thermal sink must be a very good electrical conductor to provide adequate RF grounding. When operational, two distinct thermal paths are available to remove heat from the system. An equivalent circuit model of the thermal paths is depicted in **Figure 3**. The first, and dominant, thermal path is conduction transfer through the bottom flange

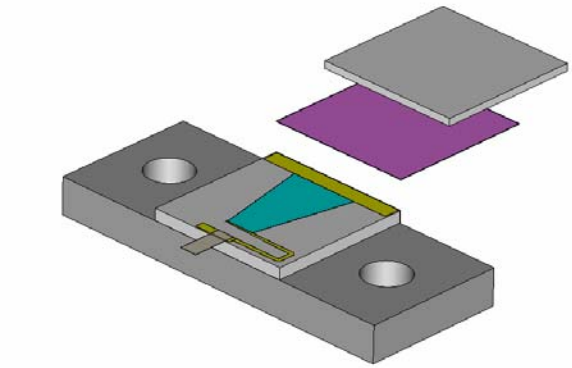

Figure 2: Open view of a flange mounted resistor

surface. The second path is through the ceramic lid via convection or conduction cooling. Using superposition theory, the two thermal paths can be treated as parallel, however, under typical operating conditions the lower thermal resistance path of the flange dominates the lid thermal path causing the thermal resistance from the active resistor area to thermal sink to be:

$$\sum\theta = \theta ss + \theta ca + \theta fl + \theta gf + \theta cbp = \mathbf{\theta jb} + \mathbf{\theta mounting}$$

If additional heat sinking through the lid is available, the equation can be modified to include the parallel thermal path. Additional heat sinking through the lid via conduction or convection cooling will increase the power handling margin of the termination.

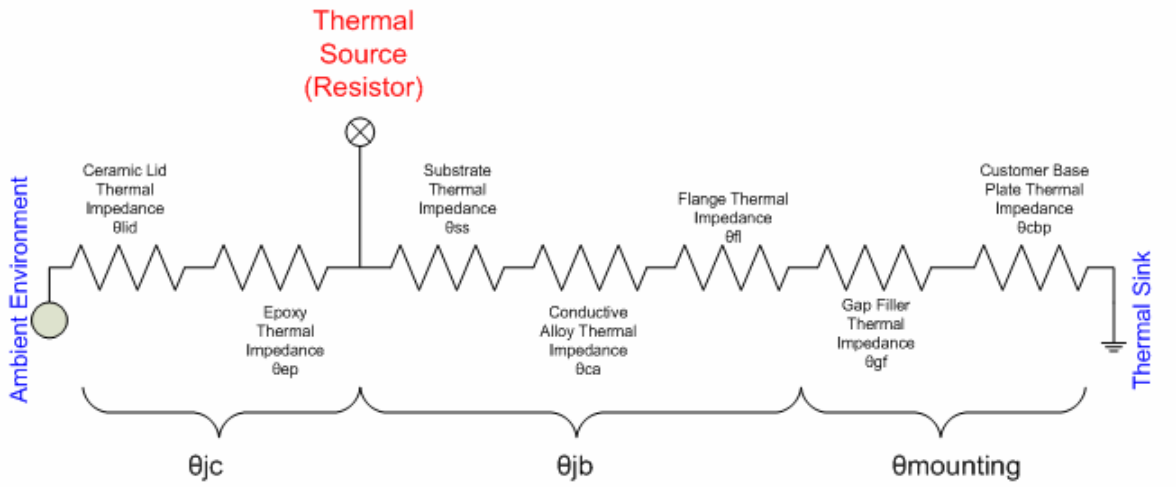

Figure 3: Thermal path equivalent circuit

As stated previously, the most efficient means of cooling the termination is conduction cooling of the flange. This is primarily due to the thermal resistance from the resistor film to the flange, θ_{jb}, being significantly less than that of the resistive path, θ_{jc}, from the resistive film to the ceramic lid. Special attention must be placed on the mounting conditions of the flange. If $\theta_{mounting}$ becomes large, the effective thermal resistance from the resistive film to the thermal sink can rise significantly causing a large ΔT between the two ($P \times \theta = \Delta T$) and could potentially damage to the resistor. When mounting flanged resistors, a very thin thermally conductive compound must be applied between the bottom surface of the flange and top surface of the customer heat sink. This will help mitigate surface contact imperfections between the flange and the customer heat sink. Air voids should not be present in this junction. Electrically conducting screws should be used to torque down the flange. This will provide enough force to maintain low thermal resistance and will also aid the integrity of the electrically conducting path to ground

Methods for Testing High Power Resistors

Testing a resistor's power handling capability can be accomplished using several different methods. The most common method is a DC power test. This test method is not the most representative test since the resistor will be exposed to RF power in application. However, during the design phase of the resistor, a correlated model can be obtained and a correlation factor can be applied to the power test results. This correlation factor will allow DC stress testing in lieu of RF stress testing.

Exposing a resistor to high power levels requires special attention during operation of the test equipment. Only qualified personnel should attempt to operate the equipment under high power levels. A common test set for DC power stress is shown in **Figure 4.**

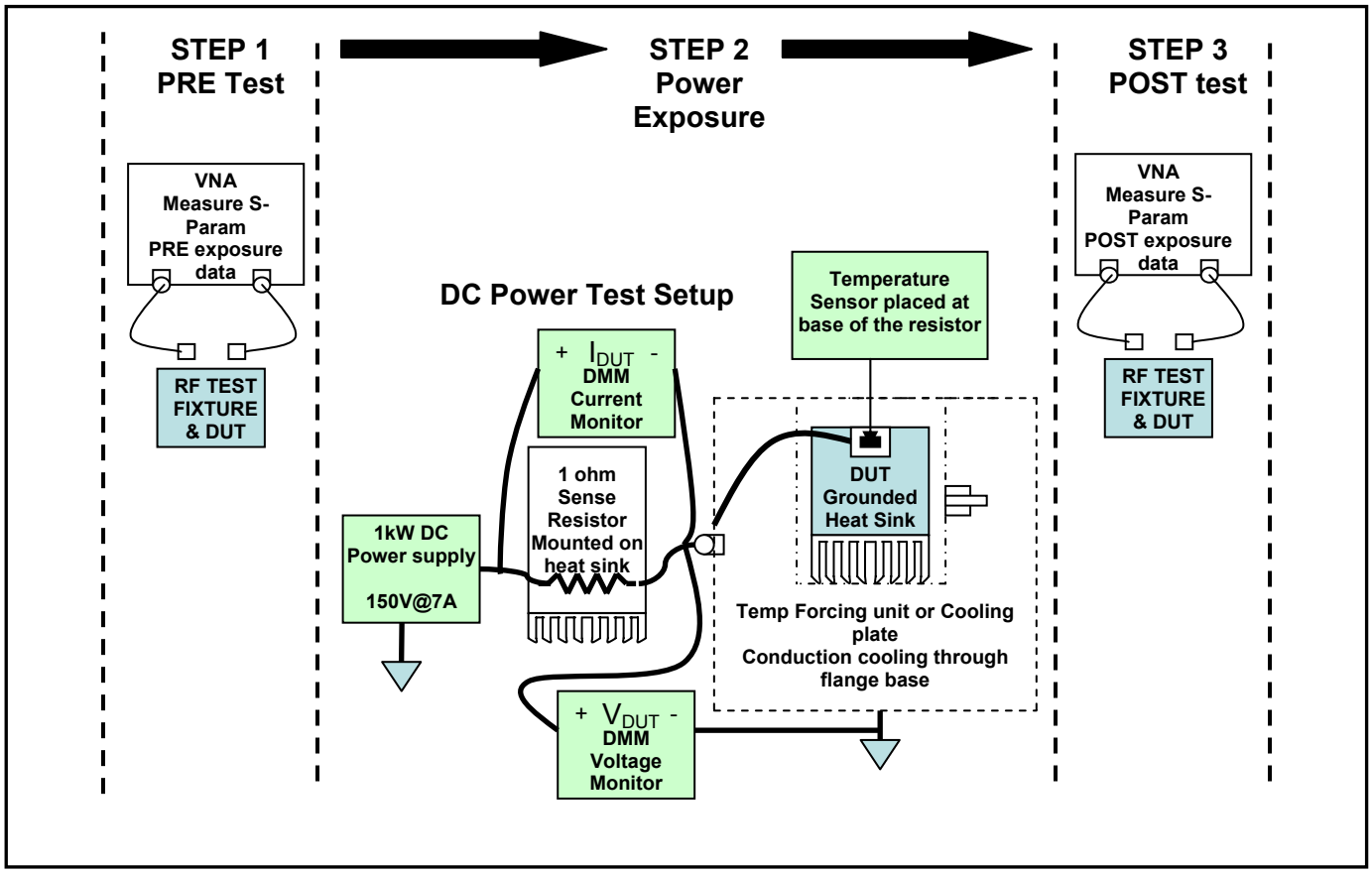

Figure 4: DC Power Test set for Termination

Qualifying a resistor requires exacting test methodologies. Resistor qualification begins with a pre-exposure S-parameters sweep as seen in **Figure 4**. This provides a baseline measurement for later comparison. Next, the resistor is subject to the power dissipation test. An appropriate power supply is used to drive the termination. The flange termination is mounted to a copper heat sink. The heat sink is either water cooled, or forced to temperature with hot/cold air. In either case, the thermal path is through the flange. See **Figure 5**. Notice the thermal grease that is used between the flange and the heat sink. This grease is used to fill in any air gaps that exist due to non-ideal surfaces of the heat sink and flange.

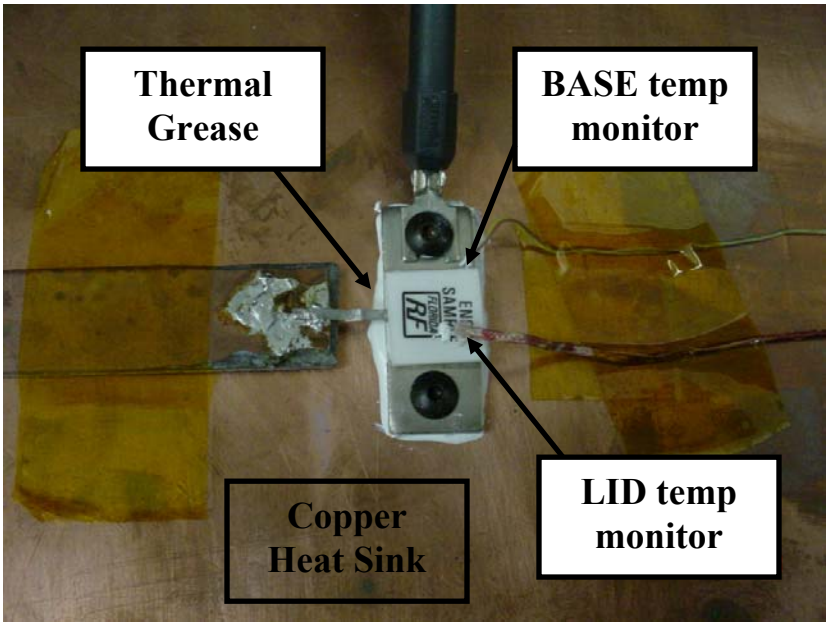

Figure 5: Termination mounted to copper heat sink

A thermal couple is placed at the intersection of the flange and the chip. Placement of the thermal couple is critical and should be at the point of highest temperature on the flange. This is the temperature controlled point during the power stress test, and is commonly referred to as the base temperature for specification purposes. Typical placement can be seen in **Figure 5**. The lid temperature depicted in **Figure 5** is also monitored during the test and is used for reference purposes. After temperature ramp up and during the "thermal soak" this point is held constant while the resistor dissipates various power levels, per the power stress test plan. The standard base temperature is specified to 100C ±3C but non-standard tests have kept this base point as high as 250C for test purposes and custom applications. This test condition is maintained for a length of time defined by the specific test plan, and is typically several thousand hours to qualify a new material or several hours to qualify a new artwork or layout. An example test data template can be seen in **Figure 6**. After the high power exposure, a post S-parameters sweep is measured and the results are compared against the pre-test data to ensure no changes in RF behavior.

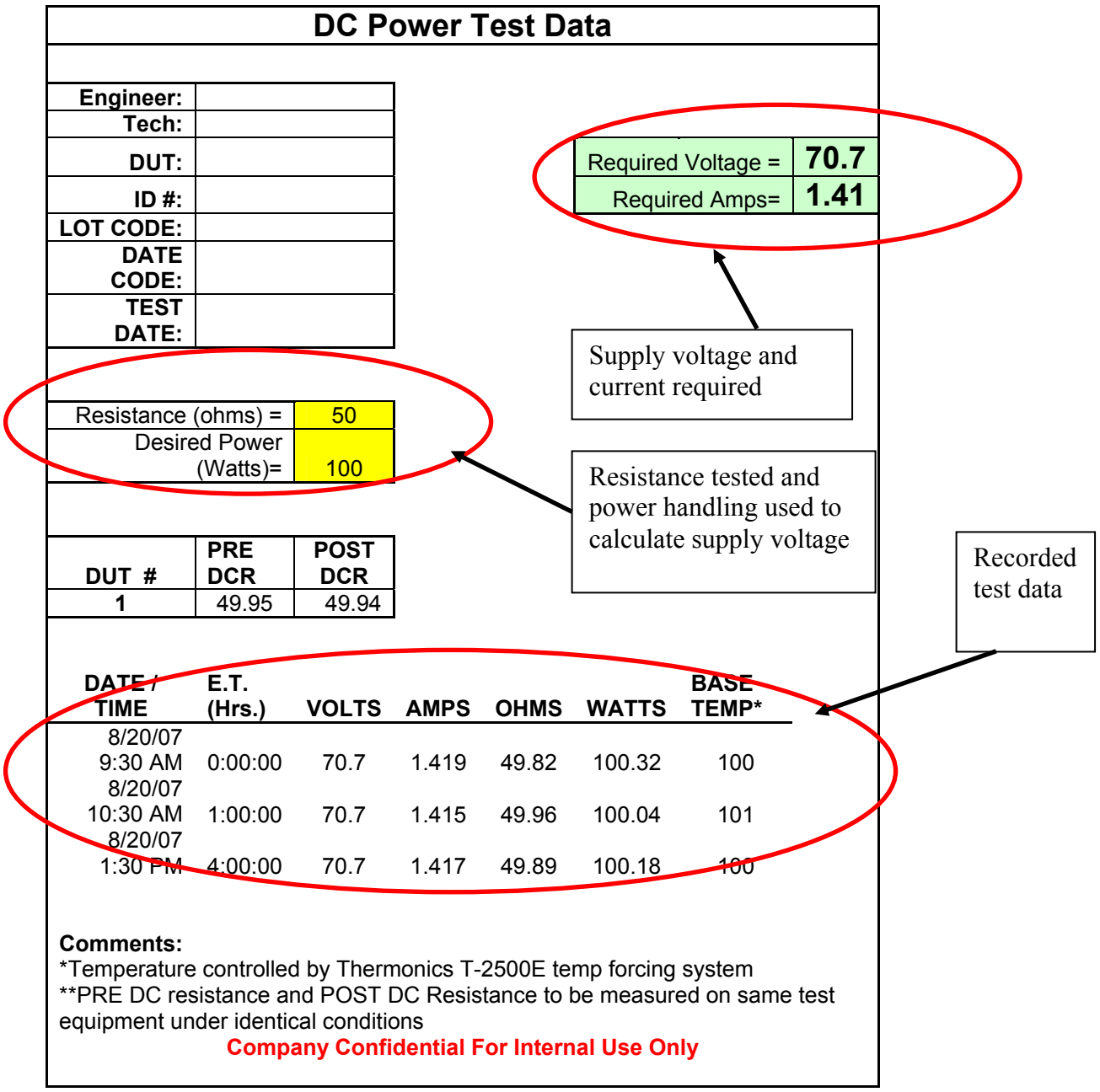

Figure 6: Power test data template

Power Specification and Derating

Power exposure testing is performed to validate the design. During the design phase of a high power resistor, a thermal model is created to ensure the thermal resistance is sufficiently low to maintain a max temperature of the dissipative element at a given power level. The power rating of the resistor is a function of several factors, but is ultimately governed by the equation $P x \theta = \Delta T$. In this equation, P is the power dissipated, θ is the thermal resistance from the resistive film to the flange surface and ΔT is the temperature difference between the resistive film and the flange surface (T_{film}-T_{base}). The industry standard for maximum allowable base temperature is 150C; however, this temperature can be increased based on the application and resistive material used to manufacture the resistor. **Figure 7** describes the industry standard de-rating and indicates the maximum operational flange temperature is 150C. An example of extended de-rating performance with a maximum operational flange temperature of 200C is in **Figure 8**. Under normal power dissipation conditions, the safe operation of a resistor is solely dependant on the resistive film temperature. Both the knee and the "x" intercept of the derating curve contain very useful information regarding the safe operation of a resistor. Refer to **Figure 8**. The base temperature at which the resistor assembly begins to derate defines the maximum, safe operational temperature of the resistive film, $T_{film\ max}$. As the dissipated power, P, approaches 0, ΔT must also approach zero to maintain balance of the equation. Considering the equation $P x \theta = \Delta T = T_{film} - T_{base}$ it is easy to determine T_{film} approaches T_{base} if 0 power is dissipated. Consequently, the base temperature corresponding to the 0 power point on the derating curve is the maximum allowable resistor film temperature!!

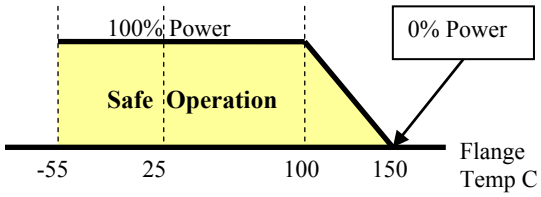

Figure 7: Industry Standard Derating Curve

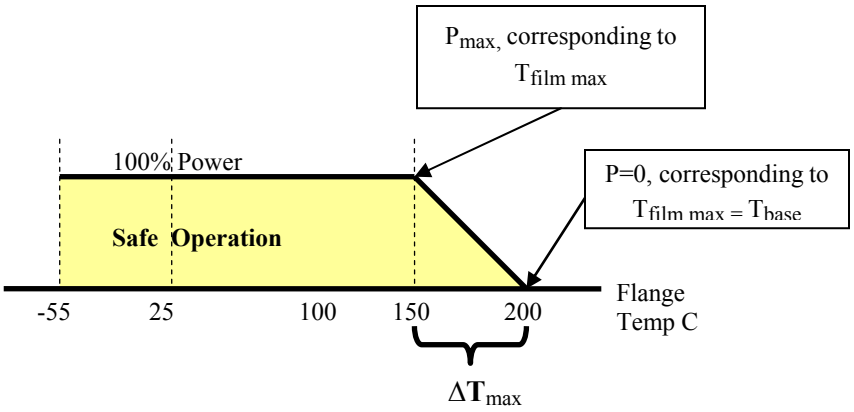

Figure 8: Example of an Extended Derating Curve

Method to Determine θjb(max)

When designing systems that utilize high power resistors, knowledge of the worst case thermal resistance from the resistive film, or the junction, to the base can aid in thermal management. This worst case thermal resistance, θjb(max), can be determined by analysis of the resistor power rating of the corresponding derating chart. By rearranging the governing thermal equation, the worst case thermal resistance from the resistive film to the base is θjb(max) = ΔT/P. For example, Florida RF Labs part number 32-1123 is rated at 350W average power at the standard derating. This equates to:

θjb(max)=50C/350W=0.143 C/W

DC Power vs. RF Power

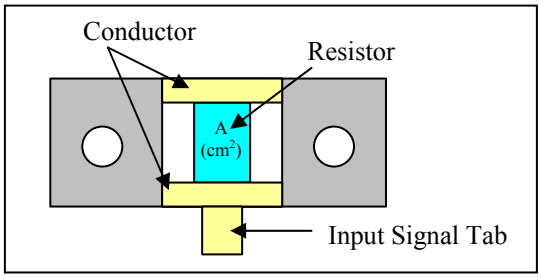

Figure 9: Termination view with lid removed

Power testing resistors typically is accomplished using a DC power source, as seen in **Figure 4**. When testing under DC conditions, the current moving through the homogeneous resistor film follows a uniform distribution for rectangular shaped resistors. The resistor is a homogenous material and will result in each ΔA of resistor area to dissipate and equivalent amount of power, ΔP. For instance, if the total average power to be dissipated is P Watts and the surface area is A cm^2 the resistor film is uniformly dissipating P/A Watts/cm^2. Thermally this resistor film acts as a uniform, surface heat generator. The rate of heat generation is the same rate as the electrical energy dissipation. DC test conditions are acceptable under this circumstance, which is if the surface current traversing the resistor is uniform throughout the resistor volume.

As the resistor's geometries become large compared to the wavelength of operation, the current density of a rectangular resistor may not be uniform and further analysis is required to validate DC test conditions. DC power dissipation may not be representative of actual RF power dissipation.

An example is illustrated below. The termination in **Figure 2** was modeled using a 3D EM simulator. The average surface current density was monitored at various frequencies and can be seen in **Figure 10**.

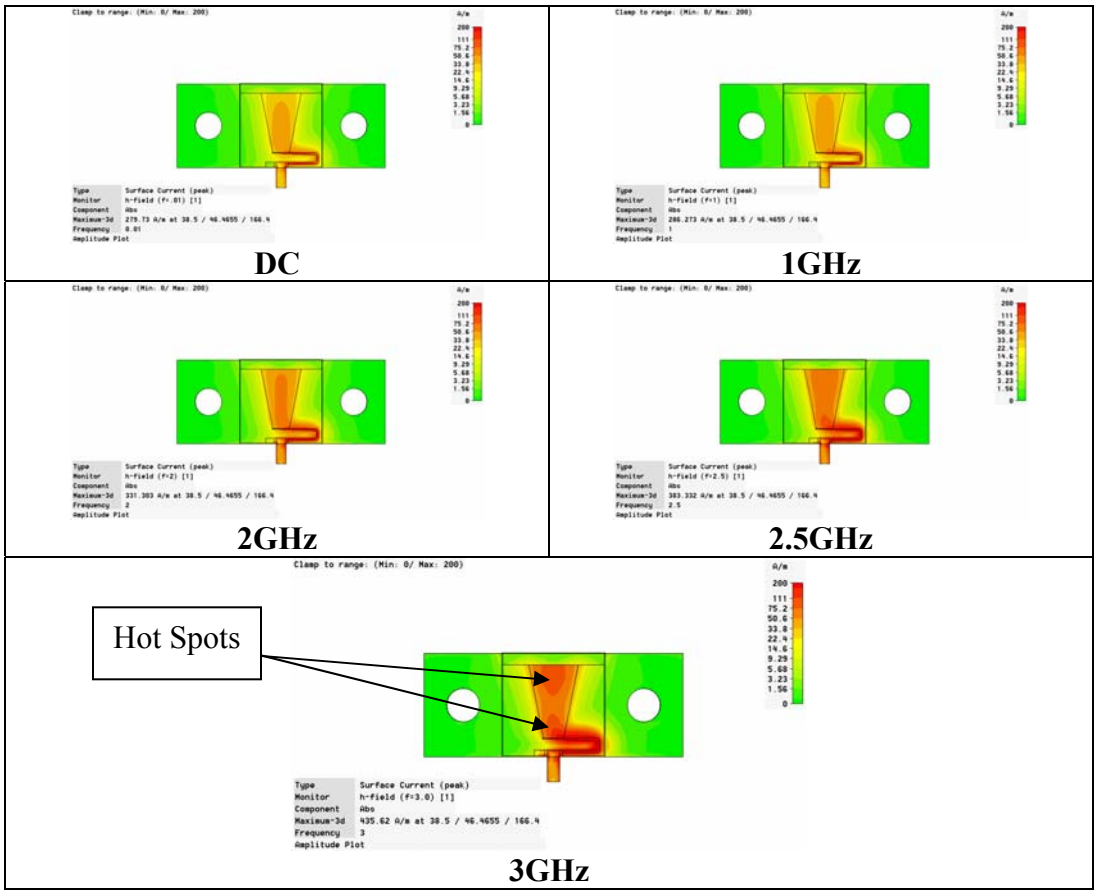

Figure 10

For the case where no time varying component of the signal exists (i.e. DC), the surface current profile is as expected with the highest current density traveling the path of least resistance. This is the path with the shortest electrical length. However, as the operational frequency increases to 2GHz and beyond, the current density distribution changes and localized "hotspots" begin to appear upon the surface of the resistor. Due to Ohmic losses, these areas of high current concentration will dissipate higher levels of energy than that of the remaining resistive film area. This results in a large, non-uniform thermal gradient across the surface of the chip which can pose thermal and/or mechanical concerns.

Pulse Power Stress

In the case of continuous wave (CW) energy dissipation in a termination, the power signal is always present and generally narrow band. The current density profile is deterministic and therefore consistent when dissipating power. Under these conditions, product reliability can be guaranteed by stressing the resistor using standard test methods. In additional to CW energy dissipation, many modern applications require very intense energy pulses to be dissipated for a short duration of time. These pulses can be random

in nature in both pulse width and repetition rate. This can cause the corresponding frequency response to be dramatically different than that of CW operation. A representative pulse waveform can be seen in **Figure 11**. This waveform is a return to zero pulse train. The Fourier transform, or frequency response, follows a sinx/x envelope. Refer to **Figure 12.** In this figure, the sinx/x response has been simplified to ease demonstration. Only the positive frequencies and the first lobe of the sinx/x response are shown. The frequency response of the sinx/x curve is governed by the pulse width, τ, and pulse period, T. "τ" will define the frequency occurrence of the first null and "T" will govern the spectral spacing of the discrete, harmonic energy content. This can be proven by analyzing the Fourier transform. Analyzing the relationship between T and τ can help draw a couple conclusions:

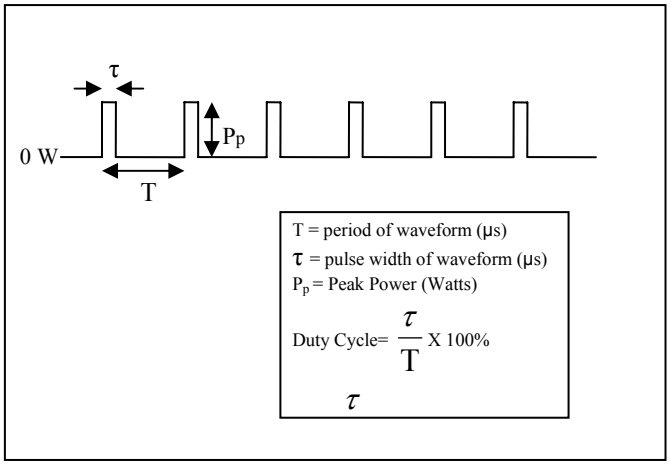

Figure 11: DC Pulse Train waveform (Return to Zero)

1. Very narrow DC pulses, spaced close together will result in a broader frequency response, with energy content throughout the spectrum at discrete frequencies. From a sinx/x perspective, this type of waveform will have the most high frequency energy content of all DC pulses trains, but still limited by "τ".
2. Wide pulses spaced further apart will have energy content contained closer to DC, with fewer discrete frequency components. This type of waveform will have the most low frequency energy content of all DC pulses trains.

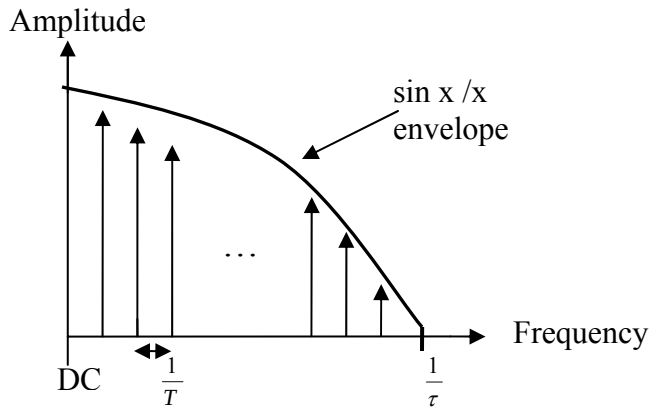

Figure 12: Frequency Response of DC Pulse Train waveform

For example, a popular DC pulse waveform with 10us pulse width with a period of 100us (10% duty cycle) will result in a frequency response contained to approximately 100 kHz (1/ τ Hz), with 10 discrete spectral components spaced by 10kHz (1/T Hz) at DC, 10 kHz, and 20 kHz through 90 kHz. This example demonstrates the popular DC pulse waveform has most energy content close to DC. One method to shift this energy to higher frequencies is through direct modulation of a CW RF source with a DC pulse train.

A modulated RF signal RF pulses will have a very distinct frequency signature. If the return to zero (RZ) pulse train in **Figure 11** modulates a CW carrier of frequency "**f_{cw}**", the operation has a multiplication effect in the time domain. See **Figure 13**.

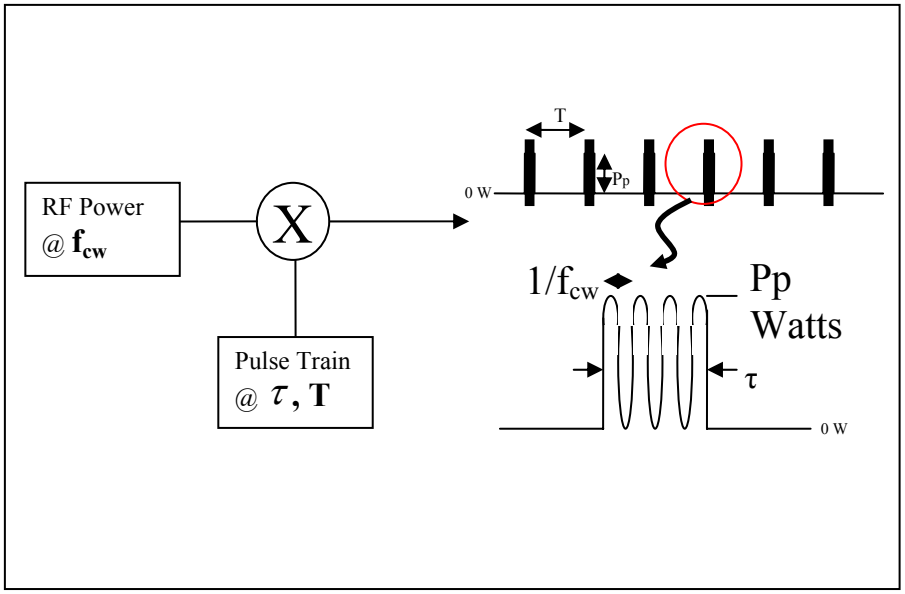

Figure 13: Modulated Signal in the Time Domain

In the frequency domain, this is equivalent to a convolution of the two spectra. This processing in effect will shift the sinx/x spectrum of the pulse train to be centered at **f_{cw}**, with some amplitude scaling. By analyzing the Fourier transform of this modulated signal, the energy content of the signal is quite different, as seen in **Figure 14**. The modulated RF signal has all energy content close to the RF source frequency, **f_{cw}**. In fact, more than 95% of the total energy is contained within $f_{cw} \pm 2/\tau$. As the pulse width, τ, increases, the modulated signal becomes more narrowband and appears to be virtually CW.

Referring back to **Figure 10,** the current density profile of the termination will vary as a function of frequency, therefore, the frequency signature of a DC pulse train and an RF modulated pulse train is different. In application, the termination can see various

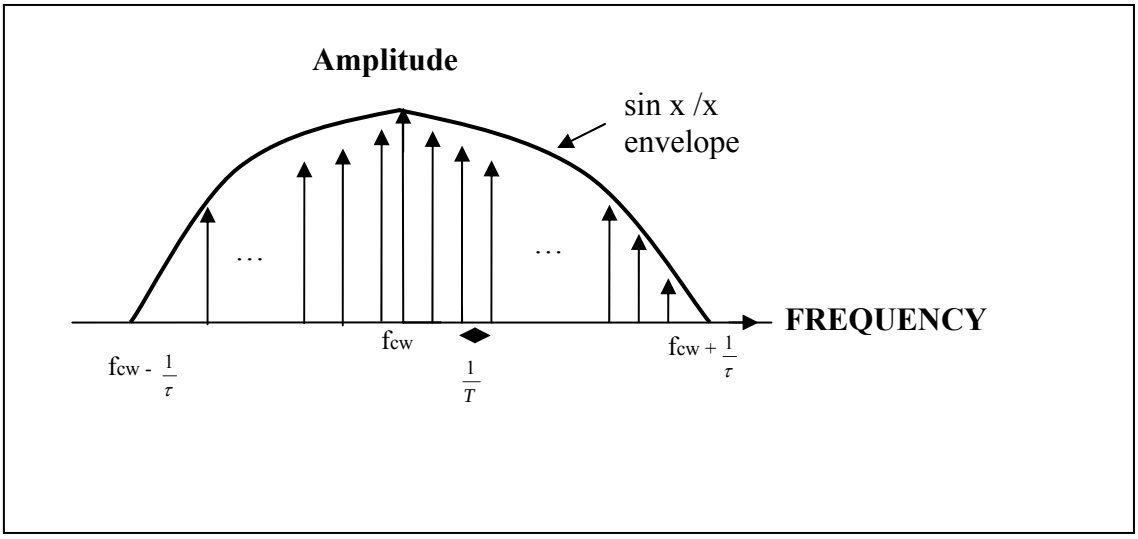

Figure 14: Frequency Response of RF modulated DC Pulse Train

waveforms with various power spectrums. Qualifying and testing the termination must be done with consideration of the frequency response, particularly for pulse applications.

Pulse Power Testing

Testing terminations or other passive products for pulse power capability is very tedious and requires experienced personnel with specific training in safety. The test set used for pulse power is very different than that of the DC test as described in the previous section (Figure 4). Monitoring the performance can no longer be accomplished using precision digital multimeters. Forward and reflected power must be monitored by means of sampling the RF energy in a directional manner. Further, the frequency spectrum must be closely monitored to ensure the required signal is applied. A descriptive block diagram is shown in **Figure 15**.

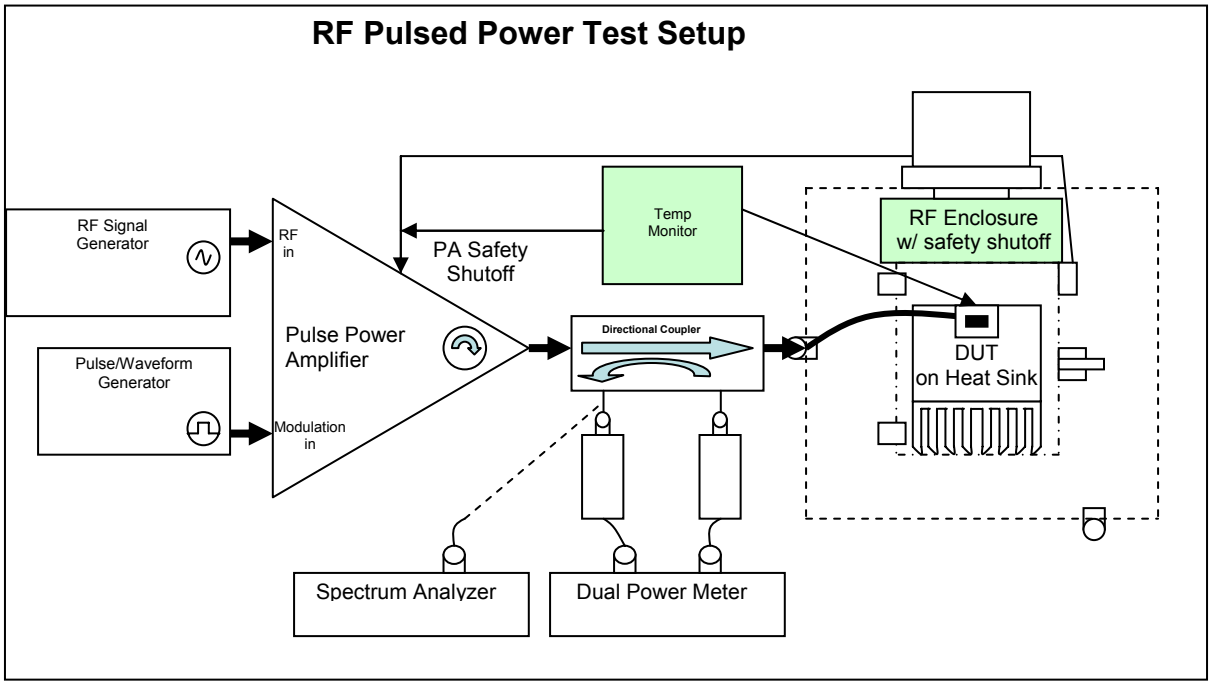

Figure 15: RF Pulse Power Test SET

Very exotic frequency spectra can be obtained by modulating the RF CW signal with an arbitrary waveform generator, which allows this test set to be customized for many applications. The limiting factor is the operating bandwidth of the pulse power amplifier. **Figure 15** depicts a test set for a termination. With some added monitoring, this same test set can be configured for high power attenuators. In this test set the Device Under Test (DUT) is mounted to a cooled plate, which works to maintain a maximum base temperature of 100C for standard test scenarios. The forward and reflected power incident to the DUT are closely monitored throughout the test and recorded to ensure proper operation. An example test data sheet can be seen below in **Figure 16**.

RF Pulse Power Test Data

Engineer:	
Tech:	
DUT:	
ID #:	
LOT CODE:	
DATE CODE:	
TEST DATE:	

Resistance (ohms) =	50
Desired Peak Power (Watts)=	3000

DUT #	PRE DCR	POST DCR
1	50	

Carrier Frequency (GHz):	1.7
Modulation waveform	Gaussian
Pulse width (us)	10
Period (us)	100

Required Peak Voltage (V) =	**387.3**
Required Peak Current (A)=	**7.75**
Required Duty Cycle=	**10.00%**
Average Power (W)=	**300**

DATE / TIME	E.T. (Hrs.)	Peak VOLTS	Forward Power (W)	Reflected Power (W)	Average Power (W)	VSWR	BASE TEMP*
8/20/07 9:30 AM	0:00:00	224	1000	25	97.5	1.05	100
8/20/07 10:30 AM	1:00:00	317	2000	48	195.2	1.05	100
8/20/07 1:30 PM	4:00:00	387	3000	72	292.8	1.05	100

Comments:

*Temperature controlled by Thermonics T-2500E temp forcing system
**PRE DC resistance and POST DC Resistance to be measured on same test equipment under identical conditions

Company Confidential For Internal Use Only

Figure 16: RF Pulse Power Test Data sheet

Summary

Florida RF Labs has provided passive power solutions for more than 20 years and has developed standard test methodologies to qualify the extensive line of power products. RF Labs offers full test services for high power products including CW power testing and pulsed power testing.